

WHAT IS CLAIMED IS:

1. A hybrid tester architecture for testing and repairing a plurality of semiconductor devices in parallel, each semiconductor device having a predetermined number of pins, the hybrid tester architecture including:
 - a computer workstation;
 - 5 per-pin formatting circuitry having data input circuitry and clock input circuitry;
 - shared timing circuitry coupled to the clock input circuitry, the shared timing circuitry operative to generate programmed timing signals; and
 - per-pin data circuitry coupled to the data input circuitry, the per-pin data circuitry operative to generate drive data associated with each individual device
 - 10 pin;whereby the per-pin formatting circuitry is responsive to the programmed timing signals to generate tester waveforms in accordance with the per-pin data.
- 15 2. A hybrid tester architecture according to claim 1 wherein:
 - the per-pin data circuitry comprises a plurality of memory blocks, each memory block corresponding to one of the predetermined number of pins.
3. A hybrid tester architecture according to claim 1 and further including:
 - a capture memory for storing fail data relating to the plurality of semiconductor devices; and
 - 5 redundancy analyzer circuitry for processing the failure data into a repair solution.
4. A hybrid tester architecture according to claim 3 wherein the redundancy analyzer is coupled to the computer workstation and operative, after generating repair solutions, to transmit the repair solutions to the computer workstation.

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5. A method of testing a plurality of semiconductor devices, each of the devices having a plurality of pins and redundant row and column addresses, the method including the steps:

- generating test data unique to each of the plurality of pins;
- 5 clocking the unique test data through unique formatting circuitry with shared timing signals;
- applying the test signals to the plurality of semiconductor devices;
- detecting and storing failure data relating to the plurality of semiconductor devices;
- 10 analyzing the failure data to generate repair solutions for activating certain of the redundant rows and columns for each of the plurality of semiconductor devices;
- routing the repair solutions back to the computer workstation; and
- programming the plurality of semiconductor devices to activate the
- 15 desired redundant rows and columns based on the repair solutions.